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What is claimed is:

1. A data processing apparatus comprising: a data input unit for input of a data; a first processing unit for processing the data inputted through the data input unit; a second processing unit for processing an output data of the first processing unit; and a display unit for display of data processed at the first and/or second processing units on a display device having a memory function, said first processing unit having a means for selectively activating the second processing unit, which has been inactivated, according to data input through the data input unit.

2. A data processing apparatus according to Claim 1, wherein the display device is a ferroelectric liquid crystal display device.

3. A data processing apparatus according to Claim 1, wherein the first processing unit has a means for detecting that the processing of the second processing unit is completed and forcedly stopping the second processing unit.

4. A data processing apparatus according to Claim 1, wherein the first processing unit has a means for driving the display unit.

5. A data processing apparatus according to Claim 1, wherein the second processing unit has a means for generation of a display start signal which instructs the first processing unit to start driving the display unit.

6. A data processing apparatus according to Claim 1, wherein the second processing unit has a means for driving

the display unit.

7. A data processing apparatus according to Claim 1, wherein the second processing unit has a means for stopping itself upon completion of its own processing action.

8. A data processing apparatus according to Claim 7, wherein the second processing unit has a means for driving the display unit.

9. A data processing apparatus according to Claim 8, wherein the second processing unit has a means for stopping itself upon completion of driving the display unit.

10. A data processing apparatus according to Claim 1, wherein the first processing unit has a means for driving the display unit and a means for delivering a display data to the display unit for change of a display state of the display unit.

11. A data processing apparatus according to Claim 10, wherein the second processing unit has a means for driving the display unit.

12. A data processing apparatus according to Claim 10, wherein the first processing unit has a means for storage of a portion of a display data of the display unit.

13. A data processing apparatus comprising: a data input unit for input of a data; a first processing unit for processing the data inputted through the data input unit; a second processing unit for processing an input data of the first processing unit; and a display unit having a memory-effect display device for display of data processed at the

first and/or second processing units, said first or second processing unit having a means for driving the display unit.

14. A data processing apparatus according to Claim 13, wherein the first processing unit has a means for activating and/or inactivating the display unit.

15. A data processing apparatus according to Claim 13, wherein the display unit has a means for inactivating itself upon completion of its display action.

16. A data processing apparatus according to Claim 13, wherein the second processing unit has a means for activating and/or inactivating the display unit.

17. A data processing apparatus according to Claim 1, wherein the data input unit has at least a keyboard of which input signal is converted by the first processing unit to a input code signal and the second processing unit has a start device remaining activated uninterruptedly and a CPU arranged for intermittent activation so that, in operation, when receiving the input code signal, the start device actuates the CPU to commence processing a program and subsequently, the CPU after completion of a desired processing action stops processing the program at a keyboard input stand-by state with its clock turned off while saving a corresponding data in its internal register and starts it again from its keyboard input stand-by state when activated by the start device.

18. A data processing apparatus according to Claim 1, wherein the second processing unit has a CPU chip containing

a register and an internal memory so that it can stop upon disconnection of a CPU clock signal with both the register and the internal memory saving data and start again when the clock signal is released.